Transregional Collaborative Research Centre 28
"Cognitive Automobiles"
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A Real-Time-capable Hard- and Software Architecture for Joint Image and Knowledge Processing in Cognitive Automobiles

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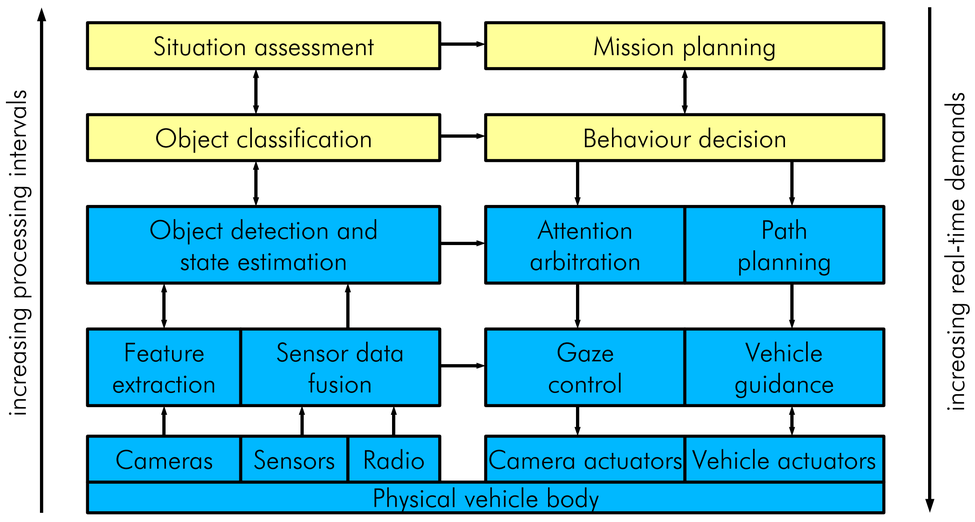
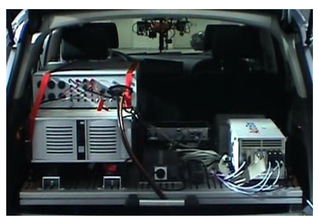
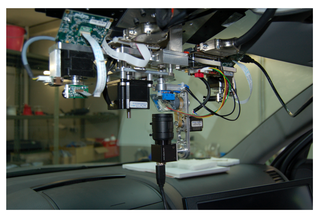
Functional Architecture

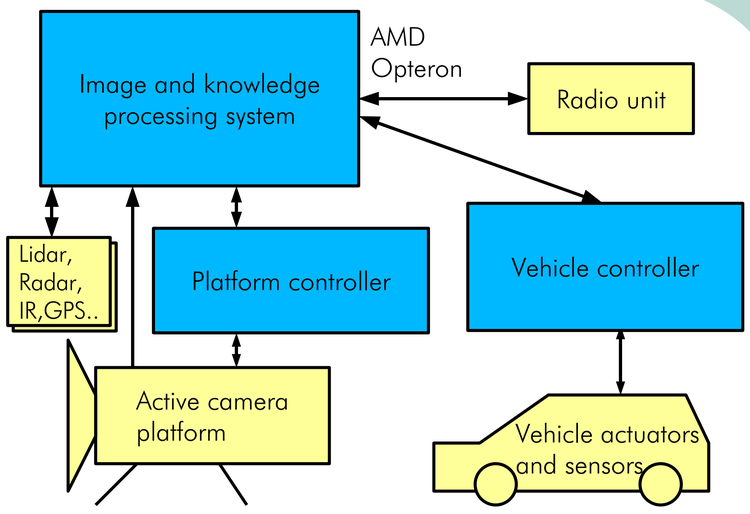
- Architectural requirements of cognitive automobiles:
  - Distinct levels of information processing with specific temporal resolutions and real-time requirements
  - Extensive information needs by all software modules for subsequent data fusion and verification
  - Combination of algorithms with different approaches
- Functional overview:



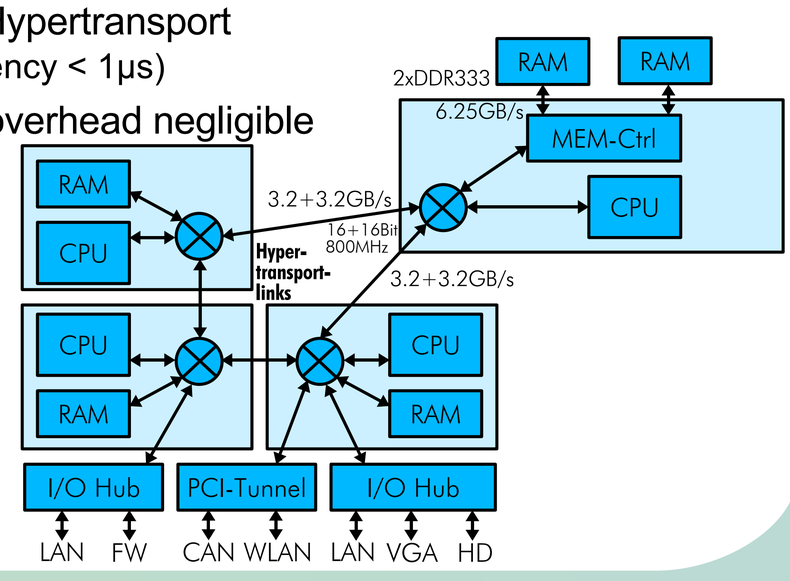
Hardware Architecture



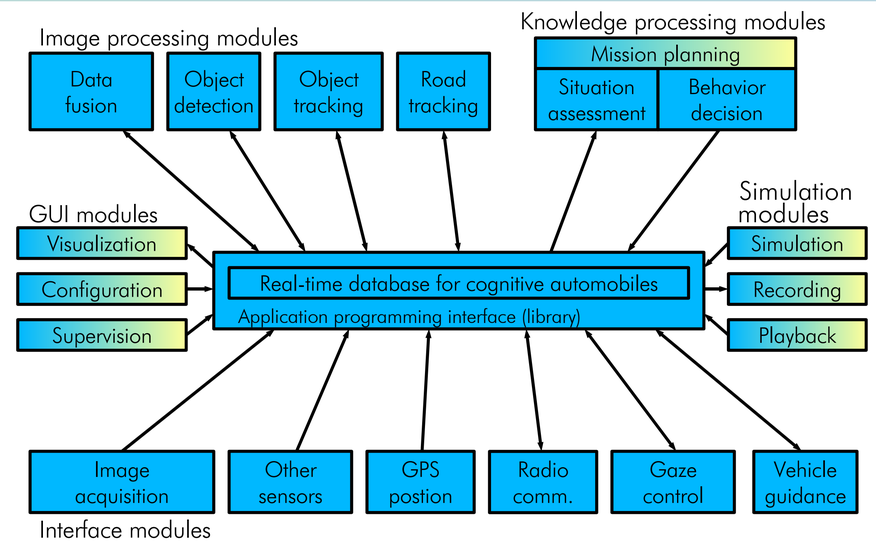




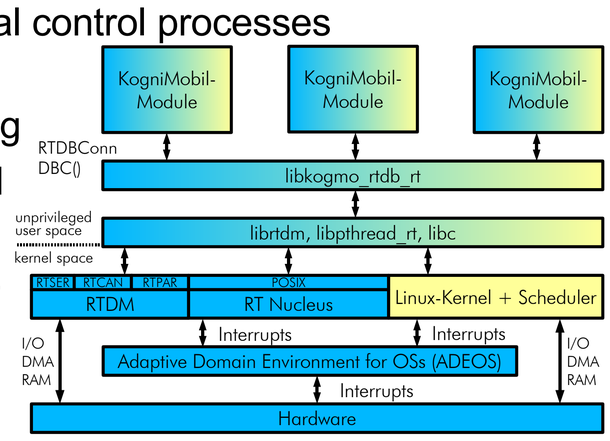
- Selected multicore multiprocessor system provides:
  - Fast computation for image processing
  - I/O bandwidth for image and sensor data acquisition
  - Large memory for knowledge processing
  - Parallel execution of cognitive functions
  - Low latencies for interprocess communication
  - Powerful storage for logging (RAID, Flash)
- AMD Opteron regarded as „Cluster-in-a-box“:
  - CPUs linked by Hypertransport ($3.2 \cdot 10^9$ byte/s, latency < 1µs)
  - Communication overhead negligible
  - Easy duplication
  - Affordable price
  - Single infrastructure components
  - 160W (2x275HE)



Software Architecture



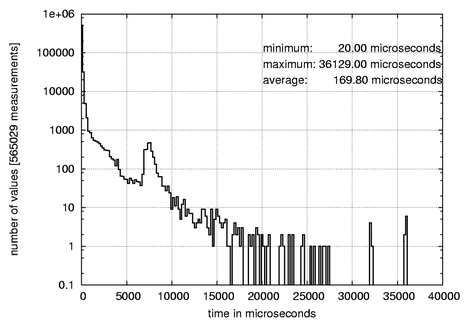
- Real-time database „KogMo-RTDB“ as integration framework:
  - Central publication of relevant information (raw sensor data, tracked objects, situation and generated behavior)
  - Open access for maximum transparency between all cognitive layers
  - Unified interface also for simulation and situation replay
  - Intuitive API that provides methods to
    - publish and update own data objects
    - search and retrieve objects from other modules
    - wait for updated data and new objects by others (trigger)
  - Temporal decoupling with history buffers and consequent use of timestamps for submitting and querying objects
  - Coherent view at the situation for slower modules
- Seamless integration of real-time and non real-time modules :
  - Hard real-time for critical control processes
  - No interference from visualisation and logging
  - Lock-less write protocol prevents blocking
  - Dynamic switch to real-time mode to prevent priority inversion



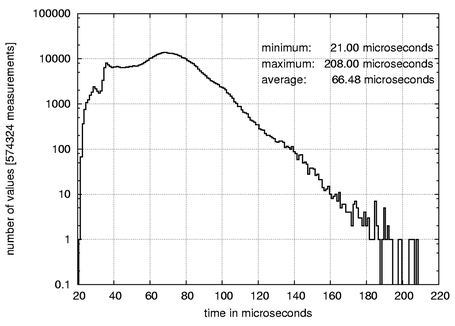
Experimental Results

- Comprehensive architecture used in several vehicles
- Powerful integration platform for tight cooperation of all cognitive modules
- Measurement results of key operations show:
  - Low overhead
  - Fast response
  - Guaranteed real-time

Operation (heavy load)	Time (average, min-max, in µs) non real-time	real-time
Insert	122.5, 39- 93109	75.6, 38-273
Delete	18.5, 4- 41250	18.5, 8-131
WriteData	22.6, 5-181681	25.6, 6-134
ReadData	17.0, 4- 10721	16.8, 4-62
IPC-Latency	169.8, 20- 36129	66.5, 21-208



Non real-time IPC latency (heavy load)



Real-time IPC latency (heavy load)

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